



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/822,512	04/02/2001	Koutaro Hachiya	Q63926	7509

7590 10/01/2004  
SUGHRUE, MION, ZINN, MACPEAK & SEAS  
2100 Pennsylvania Avenue, N.W.  
Washington, DC 20037-3202

EXAMINER

FERRIS III, FRED O

ART UNIT PAPER NUMBER

2128

DATE MAILED: 10/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 09/822,512	Applicant(s) HACHIYA, KOUTARO	
	Examiner Fred Ferris	Art Unit 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 31 May 2001.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 May 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>5/31/01</u> . | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. *Claims 1-16 have been presented for examination based on applicant's preliminary amendment filed on 31 May 2001. Claims 1-16 have been rejected by the examiner.*

### **Priority**

2. *Applicant's claim for priority based on Japanese application number P2000-102163 filed on 4 April 2000 is acknowledged.*

### **Drawings**

3. *The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "determinator" and "replacer" recited in claims 5, 6, 11, and 12 must be shown or the features canceled from the claims. No new matter should be entered.*

*Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.*

MPEP Section 608.02(d) [R-2] "Complete Illustration in Drawings" recites the following:

*"37 CFR 1.83. Content of drawing.*

*(a) The drawing in a nonprovisional application must show every feature of the invention specified in the claims. However, conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation"*

*In this case, none of the drawings (Figs. 1-17) show elements or features relating to the "determinator" or the "replacer" recited in apparatus claims 5, 6, 11, and 12.*

*Accordingly, applicants' proposed drawing corrections to Figures 1, 2 and 5 filed on 31 May 2001 have not been approved by the examiner pending correction of the issues as noted above.*

#### **Information Disclosure Statement**

4. *The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered. Specifically, page 2, line 6 of the specification references "Matrix Calculation Software", Dr. T. Kokuni, Maruzen Publishing Co. Japan, that has not been included in applicant's PTO-1492 IDS form.*

***Claim Rejections - 35 USC § 101***

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

**5. Claims 1-16 are rejected under 35 U.S.C. 101 because the claimed invention is drawn to non-statutory subject matter.** *The Examiner submits that Applicant's have not recited any limitations relating to a practical application in the technological arts and have merely claimed a manipulation of abstract ideas (mathematical constructs). Section 2106 [R-2] (Patentable Subject Matter — Computer-Related Inventions) of the MPEP recites the following:*

*“In practical terms, claims define nonstatutory processes if they:*  
*– consist solely of mathematical operations without some claimed practical application (i.e., executing a “mathematical algorithm”); or*  
*– simply manipulate abstract ideas, e.g., a bid (Schrader, 22 F.3d at 293-94, 30 USPQ2d at 1458-59) or a bubble hierarchy (Warmerdam, 33 F.3d at 1360, 31 USPQ2d at 1759), without some claimed practical application.”*

*In this case, claims 1-16 are simply drawn to the manipulation of abstract ideas (mathematical constructs - matrix reordering) as follows:*

*Claims 1-4, 7-10, and 13-16: method of matrix reordering, performing replacement of elements, and determining row and column combinations of a coefficient matrix.*

*Claims 5, 6, 11, and 12: apparatus for matrix reordering, selecting pivots, performing replacement of elements, and determining row and column combinations of a coefficient matrix.*

*An invention which is eligible for patenting under 35 U.S.C. § 101 is in the “useful arts” when it is a machine, manufacture, process or composition of matter, which*

*produces a concrete, tangible, and useful result. The fundamental test for patent eligibility is thus to determine whether the claimed invention produces a “**useful, concrete and tangible result.**” The test for practical application as applied by the examiner involves the determination of the following factors:*

*(1) “Useful” - The Supreme Court in *Diamond v. Diehr* requires that the examiner look at the claimed invention as a whole and compare any asserted utility with the claimed invention to determine whether the asserted utility is accomplished.*

*(2) “Tangible” - Applying *In re Warmerdam*, 33 F.3d 1354, 31 USPQ2d 1754 (Fed. Cir. 1994), the examiner will determine whether there is simply a mathematical construct claimed, such as a disembodied data structure and method of making it. If so, the claim involves no more than a manipulation of an abstract idea and therefore, is nonstatutory under 35 U.S.C. § 101. In *Warmerdam* the abstract idea of a data structure became capable of producing a useful result when it was fixed in a tangible medium which enabled its functionality to be realized.*

*(3) “Concrete” - Another consideration is whether the invention produces a “concrete” result. Usually, this question arises when a result cannot be assured. An appropriate rejection under 35 U.S.C. § 101 should be accompanied by a lack of enablement rejection, because the invention cannot operate as intended without undue experimentation.*

*The Examiner respectfully submits, under current PTO practice, that the claimed invention does not recite either a useful, concrete, or tangible result and is merely drawn to a manipulation of abstract ideas.*

- The invention is not **useful** since the method and apparatus of claims 1-16 does not recite a result that is useful in the technological art. This makes it difficult to determine Applicant's invention since it merely claims a*

*manipulation of abstract ideas by reordering elements of a coefficient matrix. While the preamble of independent claims 1, 2, 5, 6-8, 11 and 12 mention parallel processing and circuit simulation, the limitations of the claimed method steps merely appear to manipulate an abstract idea and do not recite a useful parallel processing or circuit simulation result. (The patent eligibility standard requires significant functionality to be present to satisfy the useful result aspect of the practical application requirement. See *Arrhythmia*, 958 F.2d at 1057, 22 USPQ2d at 1036.)*

- *The claims are not **tangible** since, for example, the results of the “replacement of elements” between rows and columns within the coefficient matrix are undefined. (see claims 1-5, for example)*
- *The claims are not **concrete** because the results are not assured. For example, is a solution possible for any and all arbitrary inputs? (i.e. any reordering or replacement of matrix elements)*

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

*To expedite a complete examination of the instant application the claims rejected under 35 USC 101 (nonstatutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them in the four statutory categories of the invention. (See 35 USC 101 rejection)*

**6. Claims 5, 6, 11, and 12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject**

Art Unit: 2128

*matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.*

*Specifically, apparatus claims 5, 6, 11, and 12 recite limitations relating to a "determinator" and a "replacer" whose structural elements (features) have not been disclosed in Figures 1-17, and, the examiner has found no teaching in applicant's specification that specifically discloses the operation of the "determinator" or the "replacer". In fact, the terms "determinator" and "replacer" do not appear to be present in the disclosure at all. Accordingly, a skilled artisan would not be able to make and/or use the claimed invention from the description of the claimed "determinator" and "replacer" contained in applicant's specification. Applicant's preliminary amendment filed on 31 May 2001 does not appear to have corrected this deficiency.*

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.



Art Unit: 2128

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

**7. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,601,080 issued to Garg in view of U.S. Patent 6,144,932 issued to Hachiya.**

Independent claims 1,2, 5-8, and 11-13 are drawn to:

method and apparatus for reordering elements of a coefficient matrix representing linear simultaneous equations produced by parallel processing using Gaussian elimination by steps of:

- based on number of non-zero elements in coefficient matrix and accumulative processing time (lengths of critical paths) of Gaussian elimination of coefficient matrix, determining (determinator: claims 5,6,11,12) a first/second combination of row and column from the coefficient matrix
- performing replacement (replacer: claims 5,6,11,12) of elements between first/second combination of row and column within the coefficient matrix. (claim 13: selecting/replacing pivots in the coefficient matrix)

Regarding dependent claims 1,2, 5-8, and 11-13: As outlined above, this group of independent claims includes the same limitations relating to a method, apparatus, and circuit simulation method for reordering the elements of a coefficient matrix representing linear simultaneous equations. These limitations are rendered obvious in view of the teachings of U.S. Patent 6,601,080 issued to Garg in view of U.S. Patent 6,144,932 issued to Hachiya. Garg discloses the elements of the claimed limitations of the present invention as follows:

- method and apparatus for reordering elements of a coefficient matrix representing

linear simultaneous equations produced by parallel processing using Gaussian elimination: Garg discloses reordering to the elements of a coefficient matrix (Abstract, CL5-L29-37, Fig. 2) that represent linear simultaneous equations (Summary, CL1-L17, CL3-L1-5, CL9-L49) and the use of Gaussian elimination (CL5-L53).

- based on number of non-zero elements in coefficient matrix and accumulative processing time (lengths of critical paths) of Gaussian elimination of coefficient matrix, determining (determiner) a first/second combination of row and column from the coefficient matrix: Garg discloses determining the number of non-zero elements in the coefficient matrix (Abstract, CL3-L5, CL5-L39) for further determining combinations of rows and columns from the coefficient matrix (CL6-L20-40, Fig. 4). Garg also discloses the use of Gaussian elimination (CL5-L53) as noted above.

- performing replacement (replacer) of elements between first/second combination of row and column within the coefficient matrix. Garg discloses the replacement (substitution) and reordering of elements (CL1-L30, CL5-L29-35, Fig. 2) between multiple (1<sup>st</sup>, 2<sup>nd</sup>, etc.) combinations of rows and columns (CL6-L20-59, Fig. 4) within the coefficient matrix (Abstract, CL3-L2)

Garg does not explicitly disclose considering the accumulative processing time or length of critical paths.

Hachiya 932' discloses simulating the operation of an electronic circuit by parallel processing and using a coefficient matrix for solving simultaneous linear equations. In

*particular, Hachiya discloses these elements while also considering the accumulative parallel processing time and the length of critical paths. (Abstract, Summary of invention, Figs. 3, 4, 7-10) Hachiya 932' discloses the elements of the claimed limitations of the present invention as follows:*

- accumulative processing time: Hachiya 932' considers the critical path execution time (processing time required) in parallel processing. (CL12-L9-39, Figs 7, 9)*
- length of critical paths: Hachiya 932' considers the communication processing over a pivot line and numerical processing increase in execution time (hence, the path length) from the broadcast of the critical combined portion (CL12-L33-39, Fig. 9).*

*Per claim 13: Hachiya further considers selecting/replacing between multiple (1<sup>st</sup>, 2<sup>nd</sup>, etc.) pivot line within the matrix (Figure 9).*

*It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Garg relating to reordering the elements of a coefficient matrix representing linear simultaneous equations, with the teachings of Hachiya 932' relating to accumulative parallel processing time and the length of critical paths, to realize the claimed invention. An obvious motivation exists since, in this case, the Garg reference teaches to the Hachiya reference, and the Hachiya reference teaches to the Garg reference. Specifically, both Garg and Hachiya teach the reordering of coefficient matrices representing linear equations used in the*

same technical arena as noted above. Garg teaches to Hachiya because Garg discloses that such methods have numerous applications including simulation of circuit design and semiconductor modeling (See: Garg CL1-L23). Hachiya teaches to Garg because Hachiya specifically discloses the use of these methods in the simulation of electronic circuits. (See: Hachiya 932': CL1-L15-39) Further, the level of skill required by an artisan to realize the claimed limitations of the present invention is clearly established by both references. (See: Garg/Hachiya, Background) Accordingly, a skilled artisan having access to the teachings of Garg and Hachiya, would have knowingly modified the teachings of Garg with the teachings of Hachiya (or visa versa) to realize the claimed elements of the present invention.

Regarding dependent claims 3, 4, 9, 10, and 14-15: These dependent claims are drawn to the additional steps of reordering (replacing) the matrix elements between combinations of rows and columns based on the symmetry of the coefficient matrix. Garg discloses matrix reordering of row and column selections based on the symmetric properties (positive-definite) of the matrix. (CL1-L20, CL5-L15-27, Fig. 2) Accordingly, as skilled artisan would have knowingly incorporated reordering features based on the symmetric properties of the matrix using the same reasoning as noted above.

Per claim 16: Hachiya further considers selecting/replacing between multiple (1<sup>st</sup>, 2<sup>nd</sup>, etc.) pivot line within the matrix (Figure 9) as previously noted above.

**Conclusion**

8. *The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, careful consideration should be given prior to applicant's response to this Office Action.*

*U.S. Patent 5,655,137 issued to Kevorkian teaches solving simultaneous linear equations using coefficient matrices and parallel processors.*

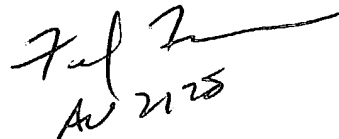
*"A New Matrix Solution Technique for General Circuit Simualtin", R. Burch, IEEE Transactions on Computer Aided Design of IC's, vol. 12, No. 2, February 1993, teaches circuit simulation using simultaneous linear equations and coefficient matrices.*

*"Parallel Programming with Control Abstraction", L.A. Crowl, ACM transactions on Prog. Lang., Vol. 16, No. 3, May 1994, teaches solving simultaneous linear equations using coefficient matrices and parallel processors.*

*Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 703-305-9670 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 703-305-3900.*

*The Official Fax Numbers are:*

Official (703) 872-9306  
*Fred Ferris*, Patent Examiner  
Simulation and Emulation, Art Unit 2128  
U.S. Patent and Trademark Office  
Crystal Park 2, Room 5D53  
Crystal City, Virginia 22202  
Phone: (703) 305 - 9670  
FAX: (703) 305 - 7240  
Fred.Ferris@uspto.gov



*Fred Ferris*  
*Art 2128*

September 24, 2004